

CMOS Fabrication Process as Utilised in Micro-Electro-Mechanical Systems (MEMS) Technology

by

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<http://www.sussex.ac.uk/profiles/9815>

Summary

- Lithography
- CMOS fabrication of an inverter
- Integrated MEMS Systems - IMEMS



TWINSCAN AT:700S - DUV step and scan

AT:700S, the first model in ASML's new TWINSCAN product line, is designed to handle 200-mm or 300-mm wafers and uses Carl Zeiss' Starlith™ 700 deep UV projection optics. This high-productivity scanning lithography tool combines innovations in system architecture and key components with the proven performance of Zeiss' Starlith optics.

Lens		Field Size	Overlay	Throughput
NA	Resolution	X & Y	2pt. Global Alignment	300mm Wafers With field-by-field leveling and 2-point global alignment. Typical exposure dose for 30mJ/cm ²
Variable 0.50 to 0.70	≤150nm	26 X 32mm	<32nm	≥62wph

Microolithography

In semiconductor manufacturing, microlithography is used to transfer the pattern of circuitry from a photomask (a quartz plate containing the "master copy" of microscopic integrated circuitry) to a wafer (a thin slice of silicon or other semiconductor material on which chips are made).

1

A tube-like cylinder of the semiconducting material silicon is cut into slices.



2

Each slice of silicon is polished to obtain an ultra-flat wafer.



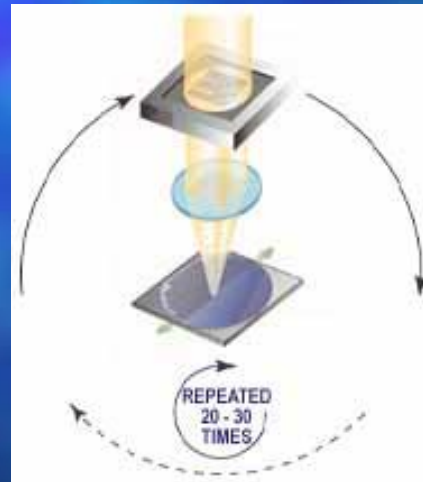
3

A thin layer of photoresist is deposited on the wafer



4

On the wafer stepper or the Step & Scan system, the lithography process is used to expose a pattern from a mask into the photoresist on the wafer.



7

Each IC is cut out of the wafer and packaged separately in a plastic frame with connectors.



6

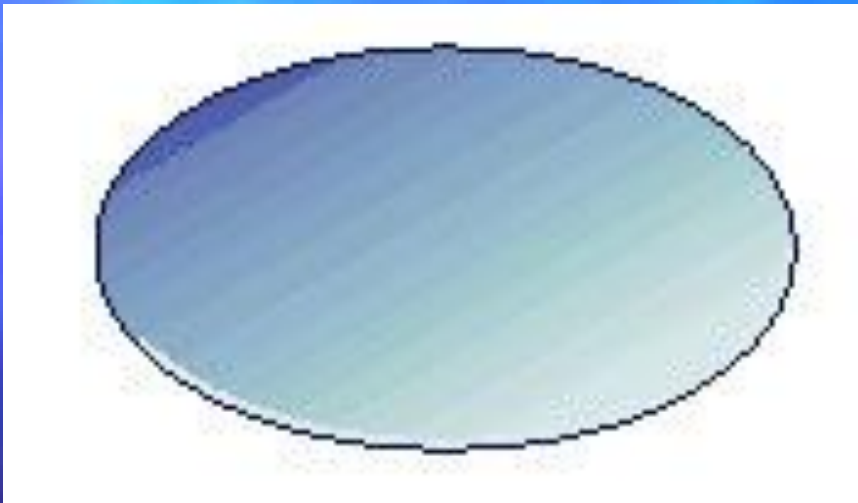
Steps 3 to 5 are repeated 20 to 30 times to build the layers necessary for the three-dimensional structure of the IC on the wafer.



5

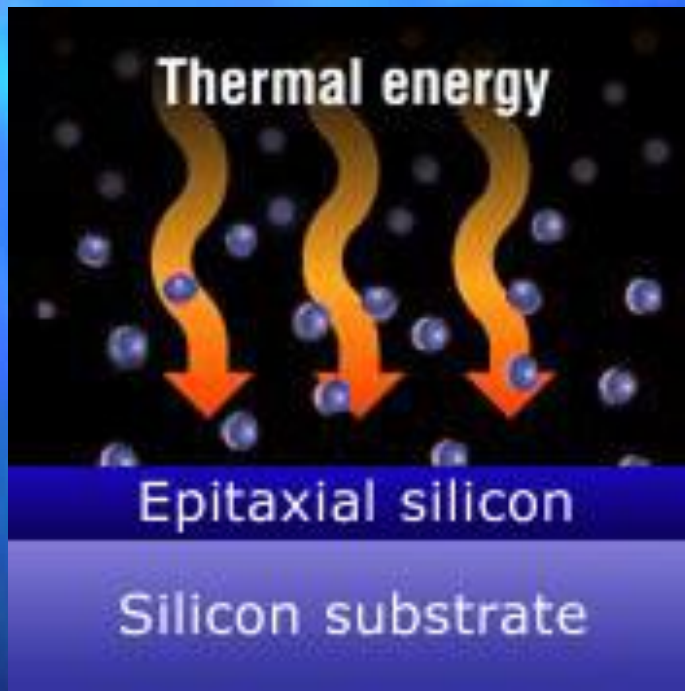
In the development process, the unexposed resist is washed away, leaving the exposed pattern on the wafer.

Silicon Wafer



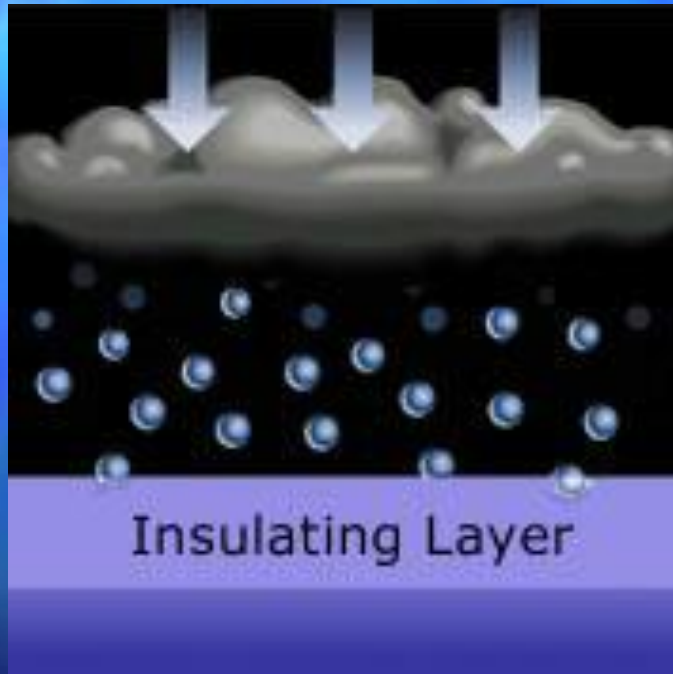
Wafers are sliced from large, cylindrical silicon crystals, then polished for use in chipmaking. Wafers are the starting point for the chip fabrication cycle.

Epitaxial Silicon



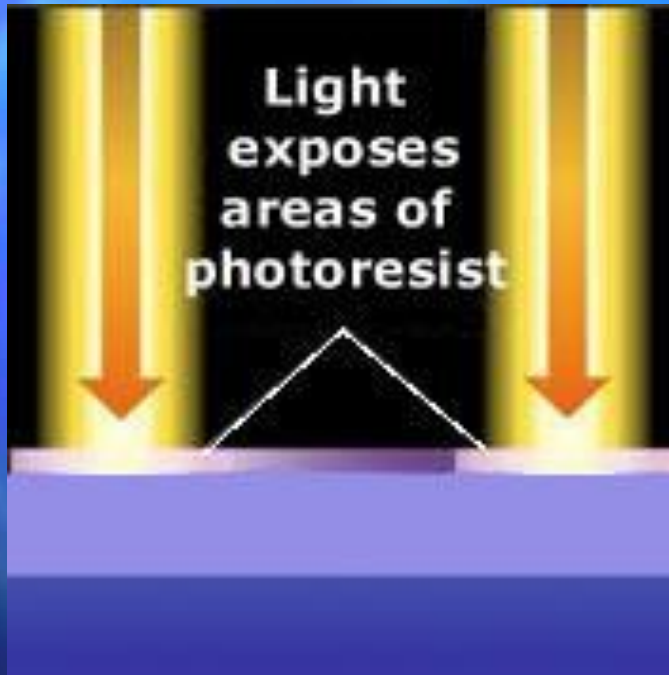
Epitaxial Silicon ("epi") is a special layer of extremely pure silicon crystal grown on some wafers to enhance chip performance.

Dielectric Deposition



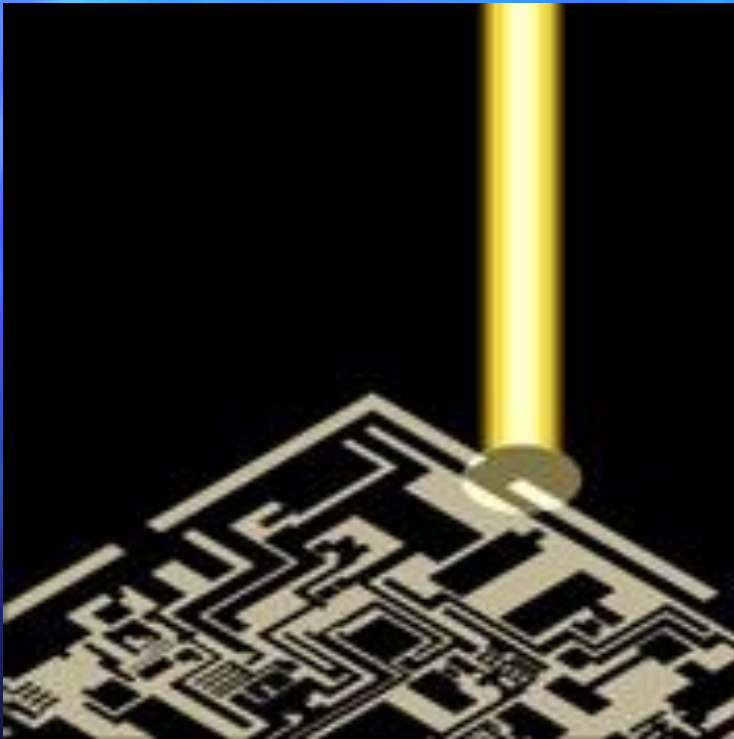
Using Chemical Vapor Deposition (CVD) technology, an insulating material is deposited on the wafer surface, forming a thin layer of solid material on the chip.

Photolithography



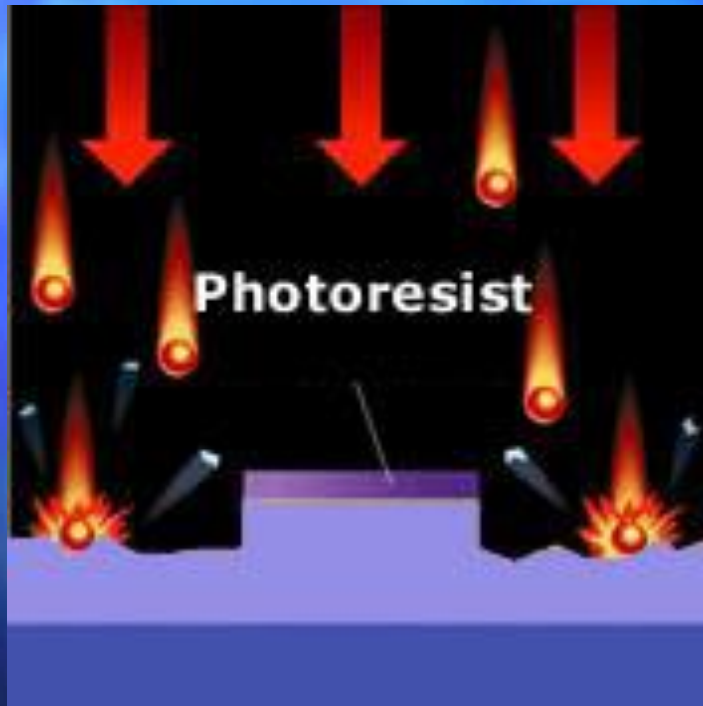
Photolithography projects a microscopic circuit pattern on the wafer surface which has a light-sensitive chemical like the emulsion on photographic film. It is repeated many times as each layer of the chip is built.

Reticle Inspection



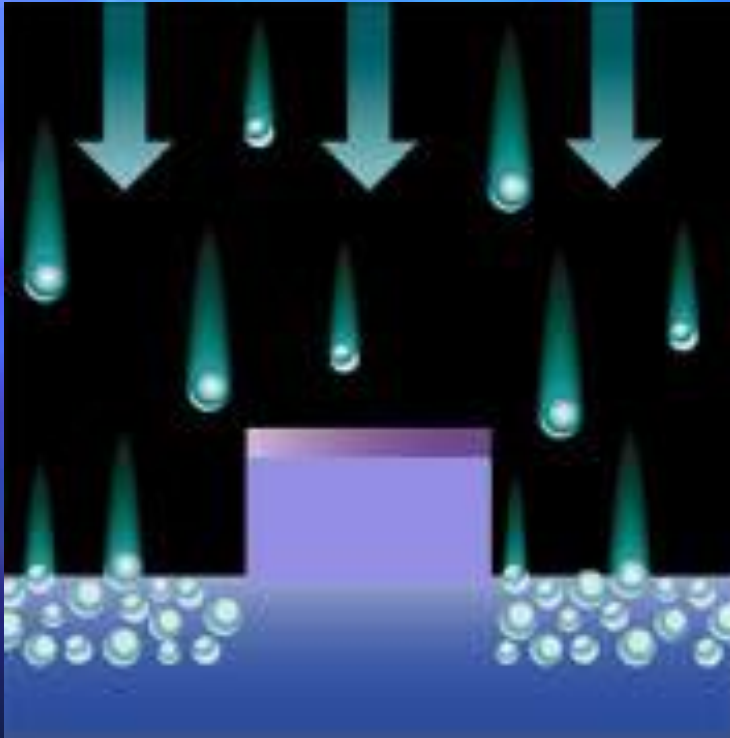
Reticle Inspection systems help ensure that the image of the circuit pattern used by the photolithography system is defect-free.

Etching



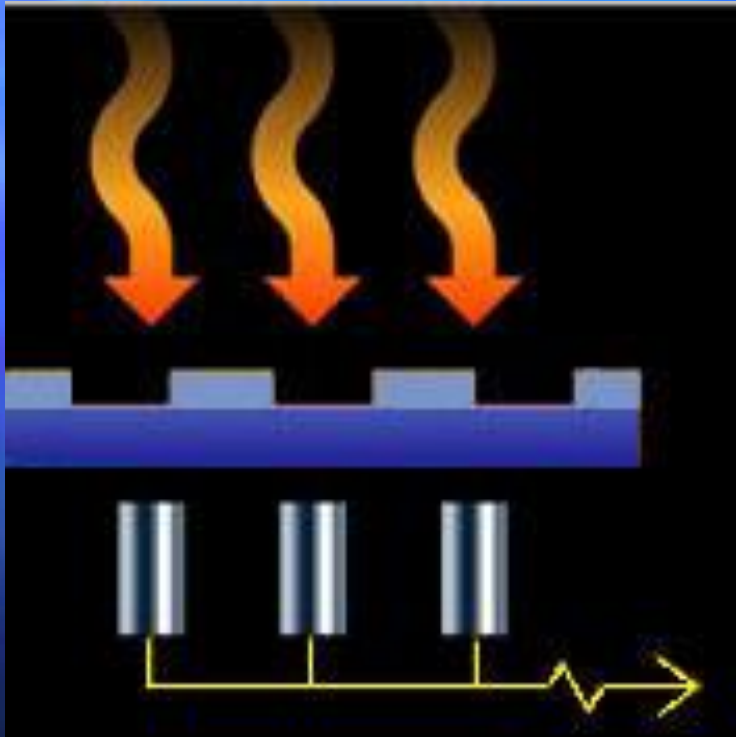
Etching removes selected material from the chip surface to create the device structures.

Ion Implantation



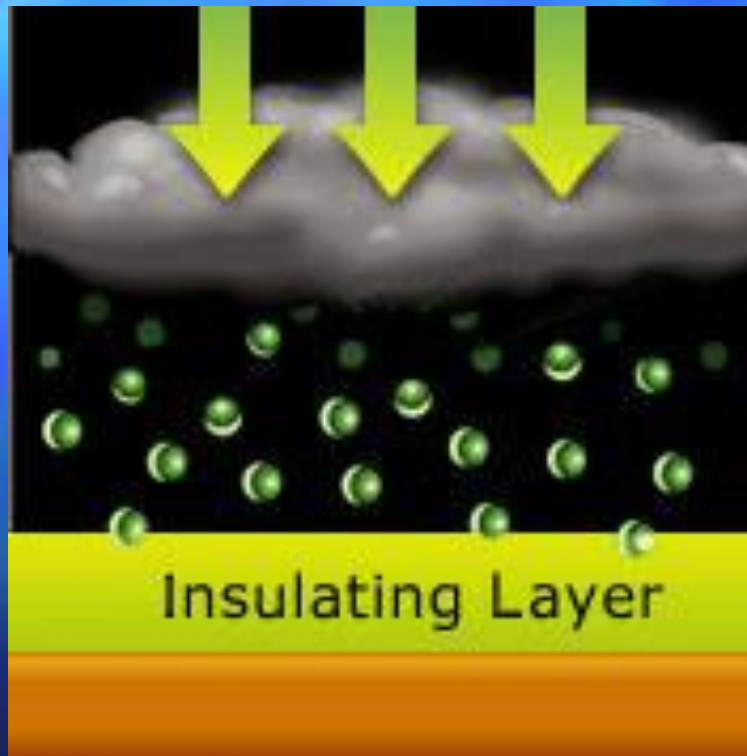
Ion Implantation accelerates “dopant” materials to a high velocity so they can penetrate (“implant”) the wafer surface and change the conductivity of the film.

Rapid Thermal Processing



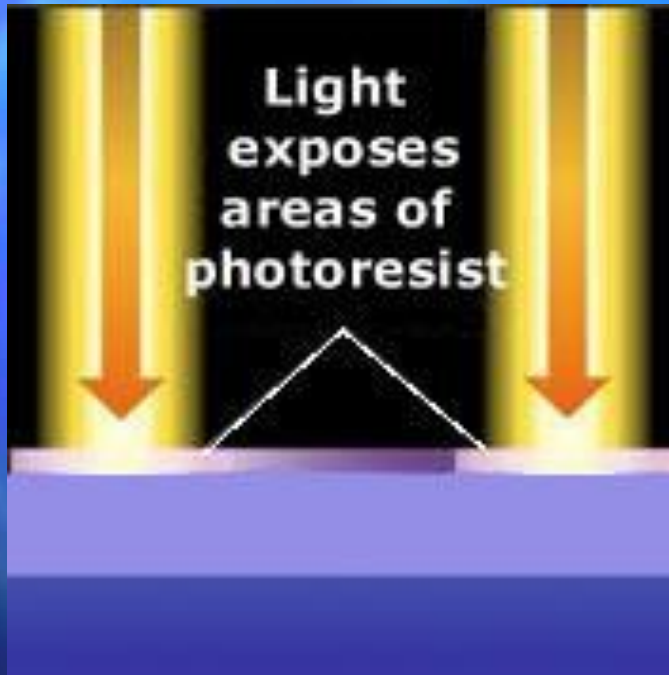
Rapid Thermal Processing (RTP) subjects the wafer to a very brief, intense burst of heat that can go from room temperature to 1000°C in seconds. This technology is used to change the characteristics of the deposited film.

Dielectric Deposition



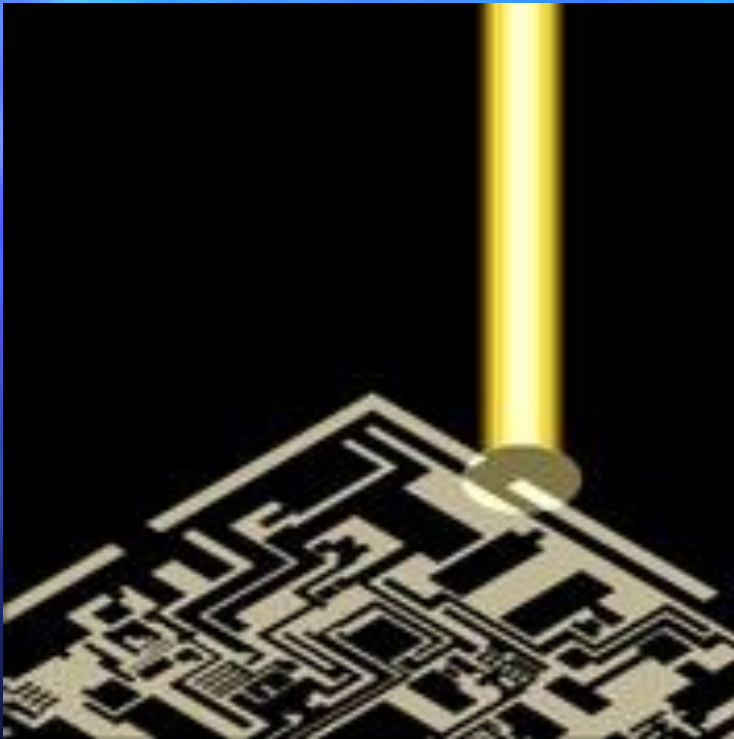
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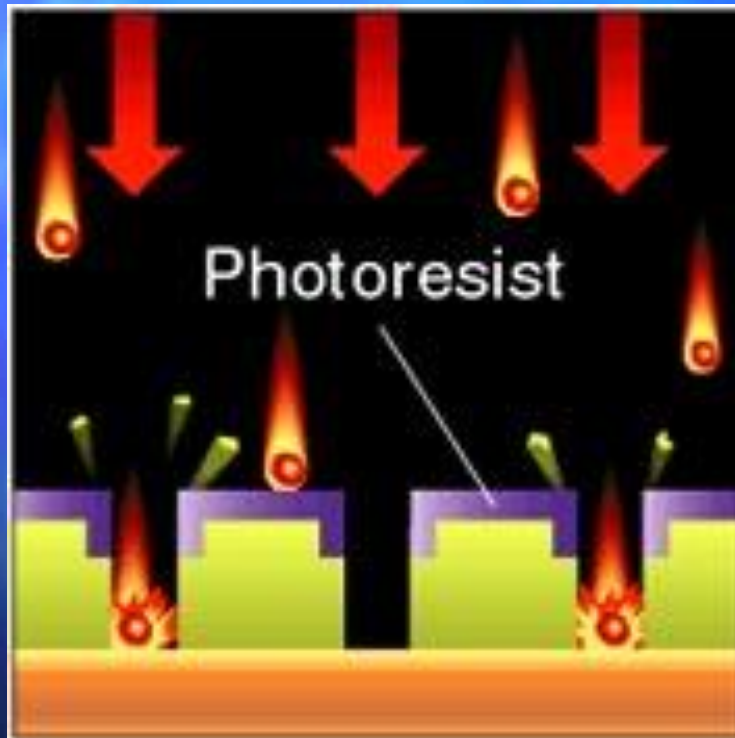
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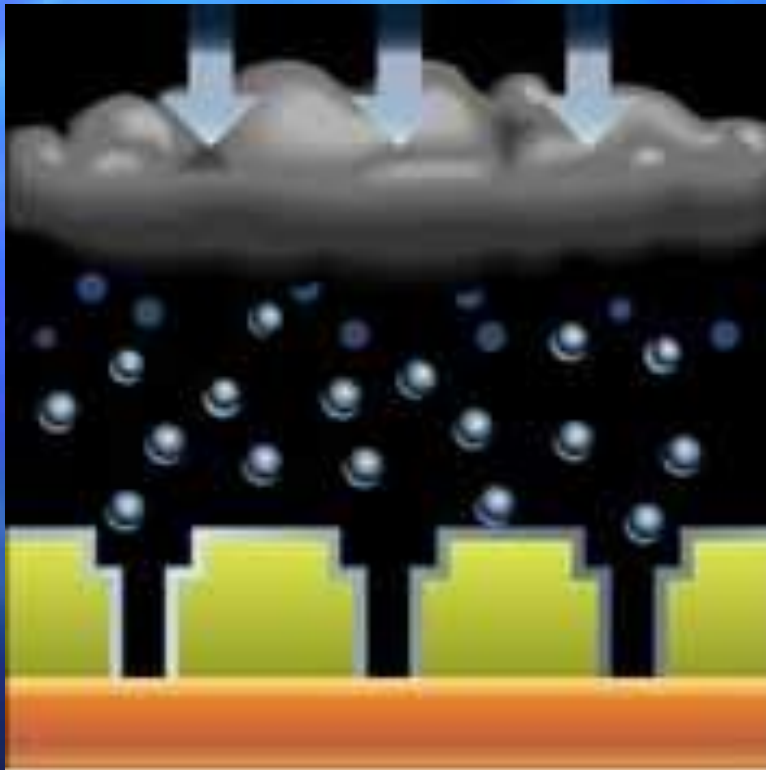
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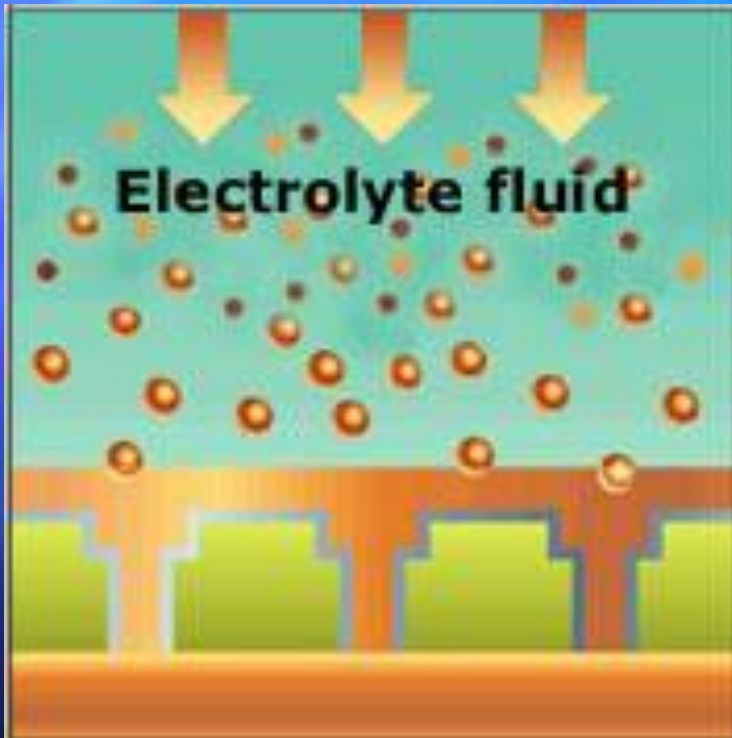
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Metal Deposition



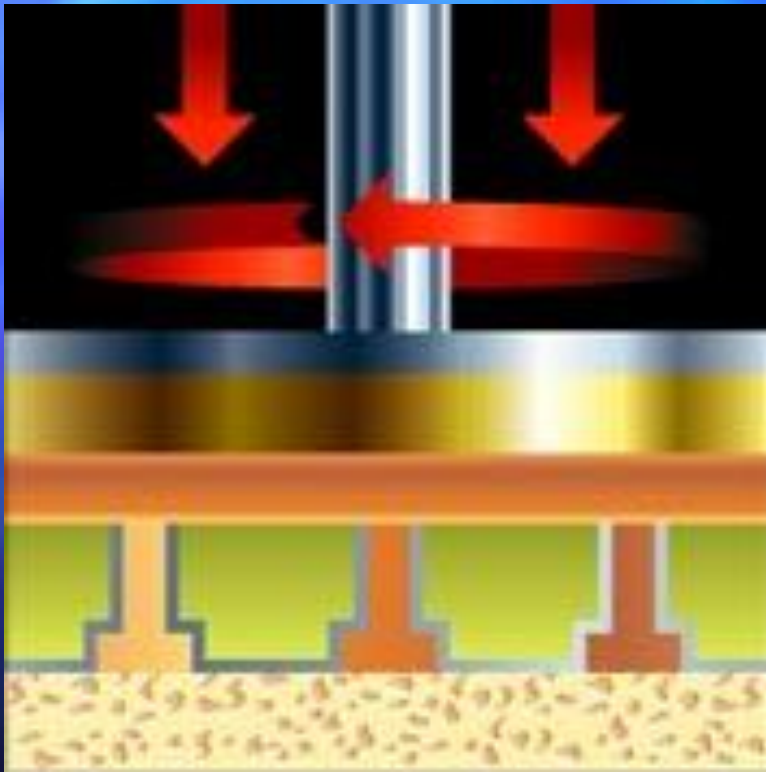
Using Physical Vapor Deposition (PVD) argon atoms are shot at a “target” of pure metal. These metal atoms then chip off and deposit on the wafer surface.

Electroplating

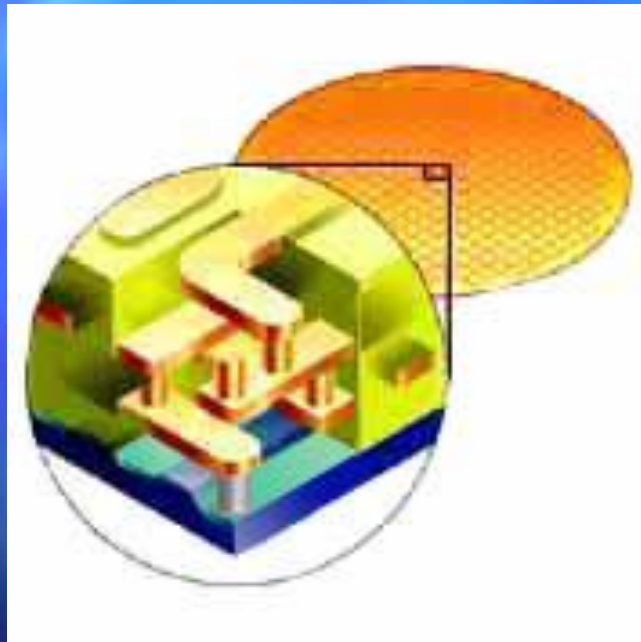


Electroplating transfers copper to a wafer immersed in a chemical solution.

Chemical Mechanical Polishing



Chemical Mechanical Polishing (CMP) combines abrasive particles in a reactive liquid solution to flatten the microscopic hills and valleys on the wafer's surface.

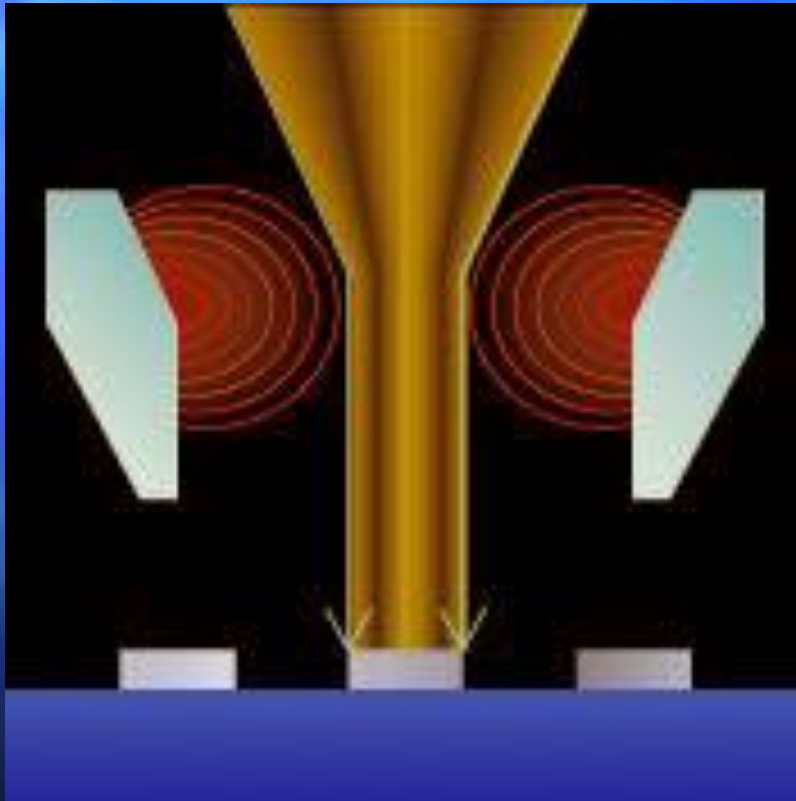


After processing, the chip is coated with a plastic or ceramic material to seal it tightly from the atmosphere.

Copper—the conductor for future chips

Copper is emerging as a new “wiring” material inside the chip. Chipmakers currently use aluminum for these wires, but copper can carry more current through the increasingly tiny circuit lines in the latest chip designs. The use of copper will allow faster, more powerful chips.

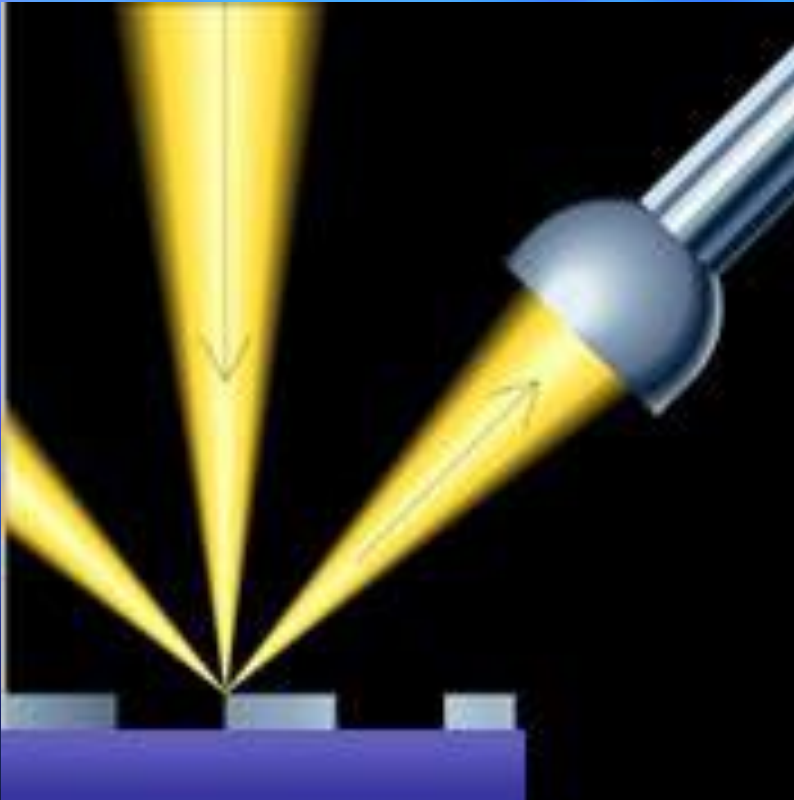
SEM Metrology & Inspection



Scanning Electron Microscopes (SEMs) measure the size of circuit features at very high magnification to check the accuracy of the manufacturing process.

Other types of SEMs review and classify defects on the wafer—such as particles or scratches—in order to help find their source.

Defect Detection



Defect Detection systems identify possible defects on wafers as they move between processing steps.



Silicon Etch DPS Plus Centura

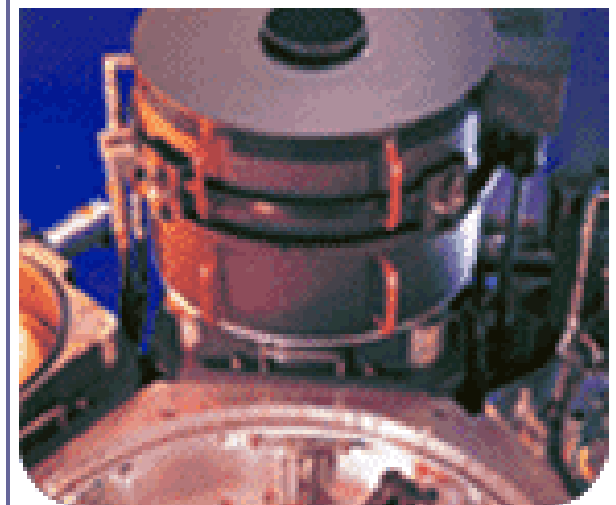
High-productivity sub-0.15 μ m silicon dry etching for transistor and gate formation

Metal Etch DPS Plus Centura

Advanced interconnect formation with the industry's lowest cost-per-wafer metal dry etching



Dielectric Etch eMAX™ system



Aluminium and Copper Inter-connect



Endura SL – Cu/Al



Electra™ Cu ECP - High Volume



Endura® Aluminum Interconnect



Endura® Electra Cu™ Barrier/Seed



Rapid Thermal Processing (RTP)

RTP was originally developed to address implant anneals and the formation of silicides. Later these processes spread to include oxidation and nitridation. Oxidation occurs when the wafer is heated very quickly in oxidizing gases to form silicon dioxide layers on the wafer surface.



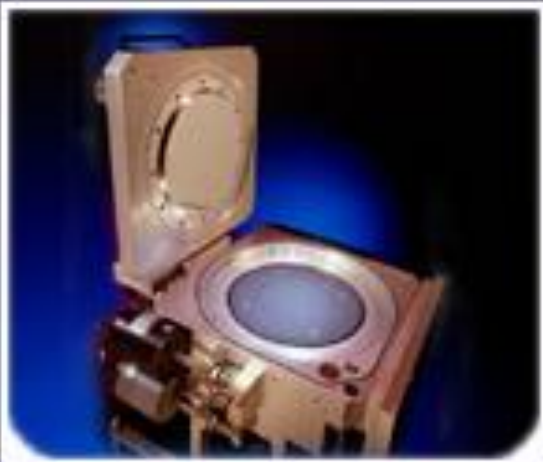
Sub-Atmospheric Chemical Vapor Deposition (SACVD)

Using TEOS (tetraethylorthosilicate) and Ozone (O_3) chemistry at near-atmospheric pressure, SACVD quickly proved its ability to achieve excellent step coverage, void-free gap-filling and superior planarization characteristics in high aspect ratio structures down to 0.25 micron with high throughput and reliable operation.



Reflexion™ 300mm CMP

The Reflexion system is Applied Materials' 300mm CMP platform. The Reflexion system offers 300mm processing capabilities for oxide, STI, polysilicon, tungsten, and copper applications.



Low Pressure Chemical Vapour Deposition (LPCVD)

Polysilicon and silicon nitride are deposited using low-pressure CVD, or LPCVD, batch systems such as horizontal or vertical furnaces.



Ion Implantation

9500xR energy ranges of 2 to 750 kilo-electron volts, or "keV."

PAS 5500/1100



PAS 5500/1100 193 nm Step & Scan

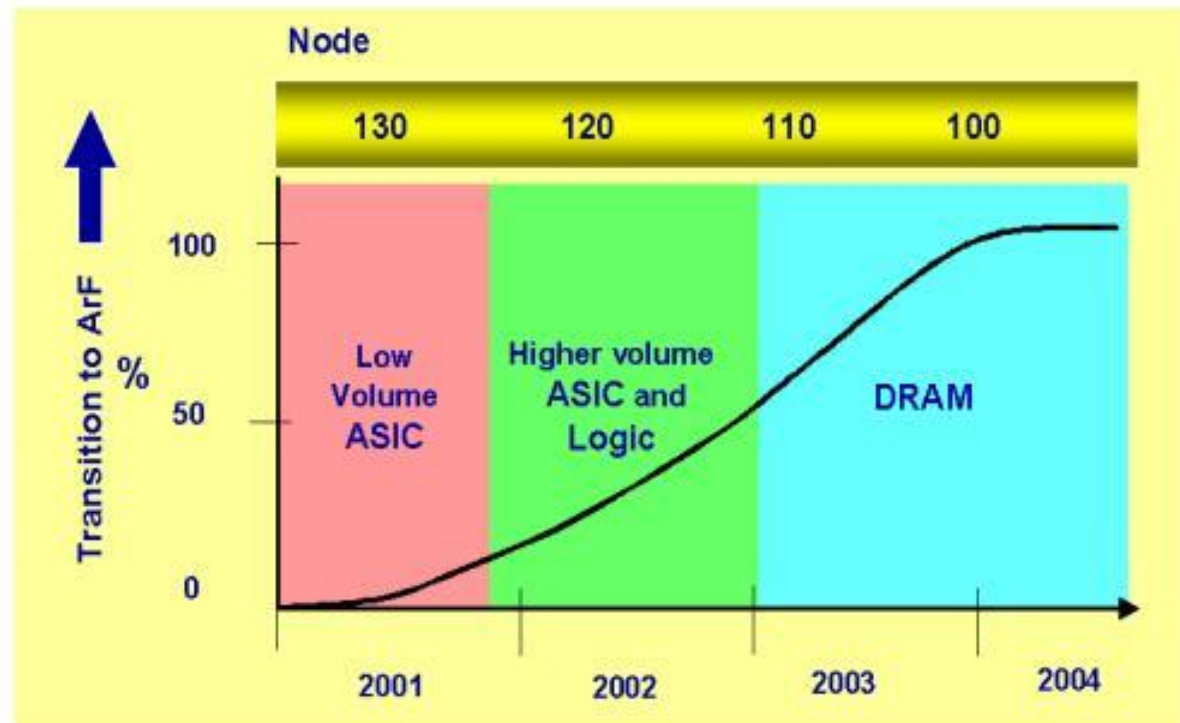
The solution for
volume production
@ 100 nm !!!

PAS 5500/1100 introduction
November 2000



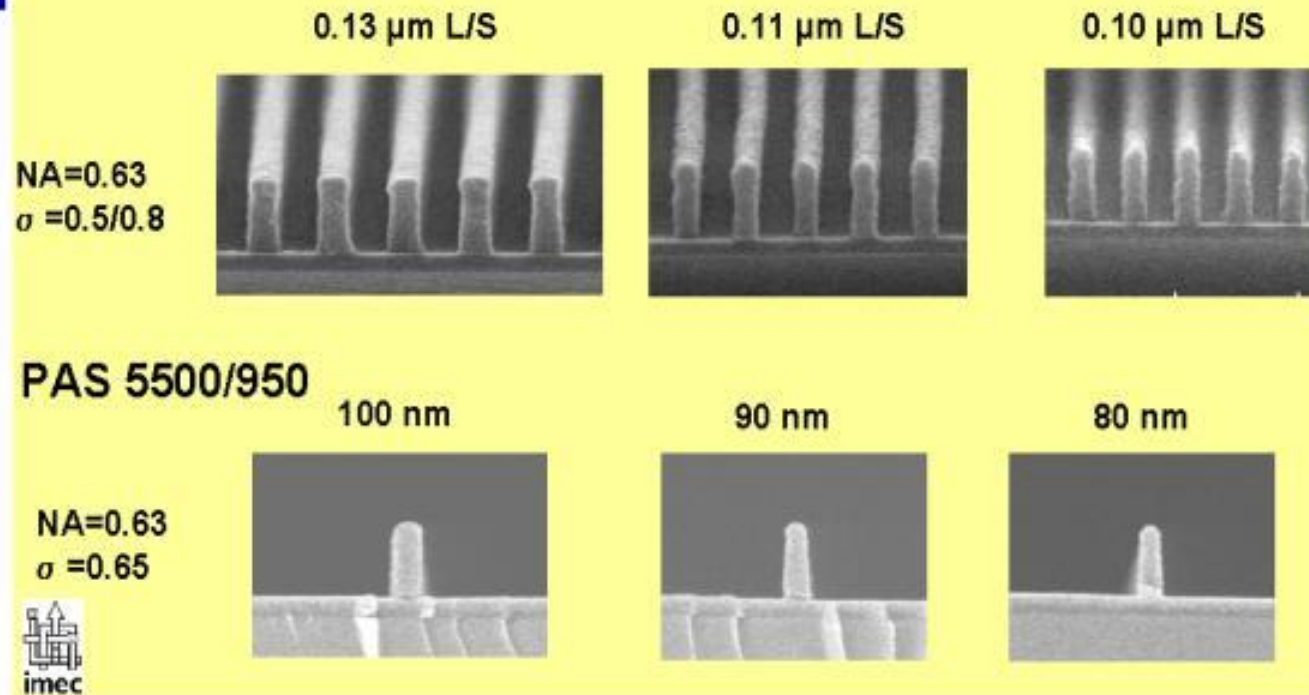
The PAS 5500/1100 Step & Scan tool utilizes Carl Zeiss' new Starlith™ 1100 lens, whose 0.75 NA matches the industry's largest. High-quality optical materials and coatings result in high transmission of 193nm-wavelength light. The illumination source is a 2 kHz, 10 W laser with a bandwidth of 0.35 pm.

Market Transition KrF to ArF



PAS 5500/1100 introduction
November 2000

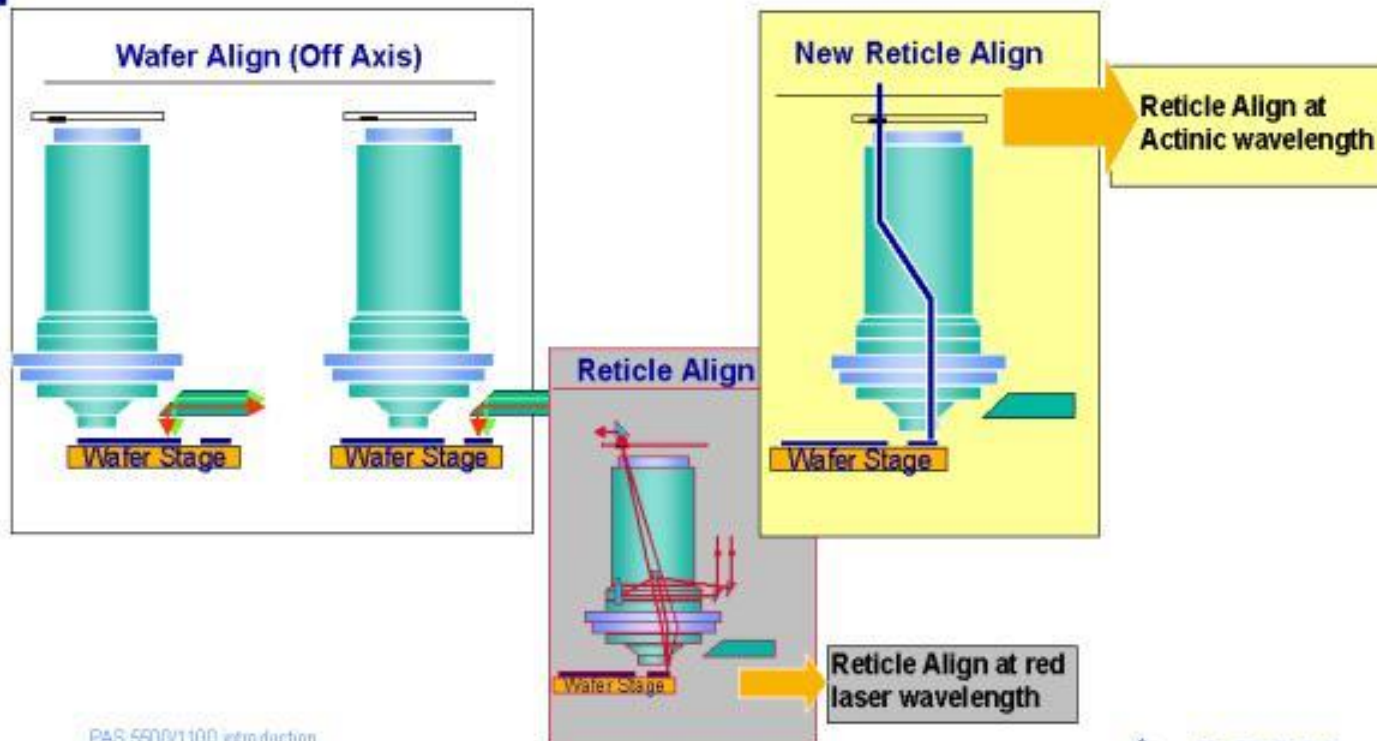
■ Resolution of advanced 193 nm resist



PAS 5500/1100 introduction
November 2000

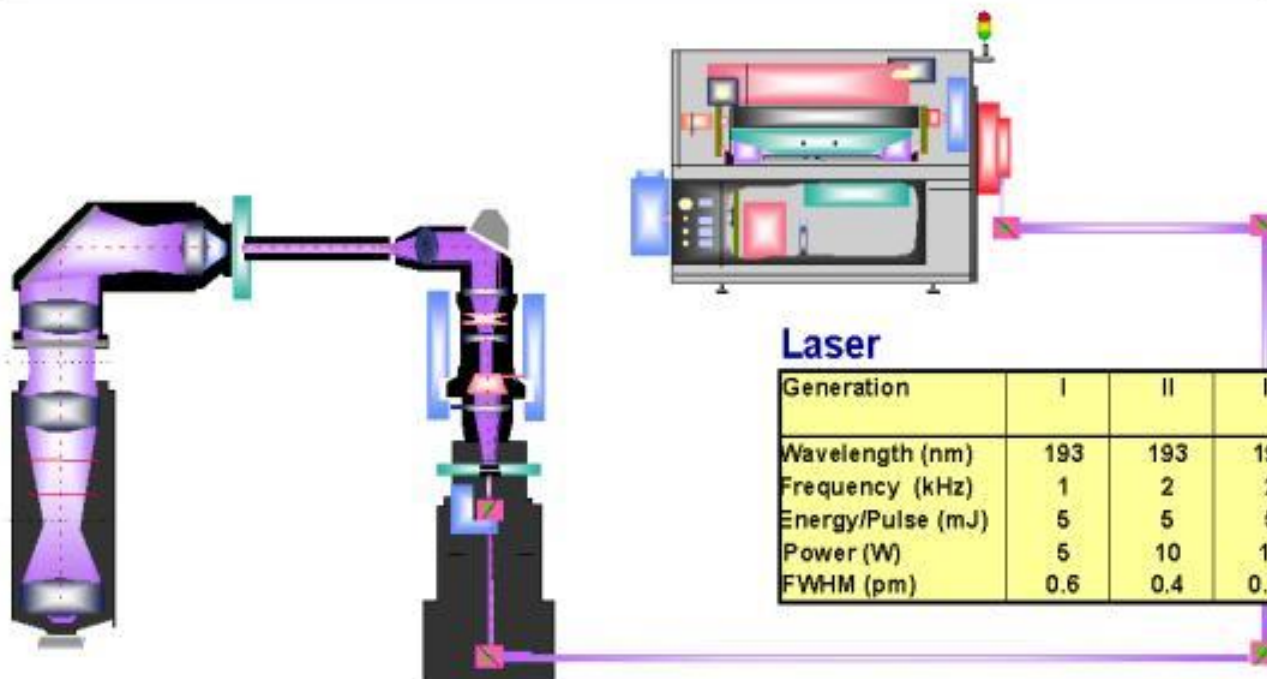
New Reticle Align at Actinic Wavelength

Sequence to Align Wafer and Reticle



PAS 5500/1100 introduction
November 2000

Laser



Laser

Generation	I	II	III
Wavelength (nm)	193	193	193
Frequency (kHz)	1	2	2
Energy/Pulse (mJ)	5	5	5
Power (W)	5	10	10
FWHM (pm)	0.6	0.4	0.35

5500/1100 Summary of Specifications

Lens Specifications		AERIAL™ II Illuminator	
Wavelength (nm)	193	Sigma range	0.25 - 0.88
NA	0.75→ 0.50	Overlay Specifications	
Resolution L/S (nm)	≤ 100	Overlay (nm)	≤ 25
Reduction	4X		
Field Size			
Max X, Y (mm)	26, 32	Throughput @ 20 mJ/cm²	
Laser		Wafer layout with 46 exp	≥ 90 wph
2 kHz, 10W, 0.35 pm Bandwidth			



CMOS FABRICATION PROCESS

Periodic Table of the Elements

1 IA New Original												18 VIIIA						
1 H Hydrogen 1.00794	2 He Helium 4.002602											3 Li Lithium 6.941	4 Be Beryllium 9.012182					
5 B Boron 10.811	6 C Carbon 12.0107	7 N Nitrogen 14.00674	8 O Oxygen 15.9994	9 F Fluorine 18.9984032	10 Ne Neon 20.1797	11 Na Sodium 22.989770	12 Mg Magnesium 24.3050	13 Al Aluminum 26.981538	14 Si Silicon 28.0855	15 P Phosphorus 30.973761	16 S Sulfur 32.066	17 Cl Chlorine 35.453	18 Ar Argon 39.948					
19 K Potassium 39.0983	20 Ca Calcium 40.078	21 Sc Scandium 44.955910	22 Ti Titanium 47.867	23 V Vanadium 50.9415	24 Cr Chromium 51.9961	25 Mn Manganese 54.938049	26 Fe Iron 55.8457	27 Co Cobalt 58.933200	28 Ni Nickel 58.6934	29 Cu Copper 63.546	30 Zn Zinc 65.409	31 Ga Gallium 69.723	32 Ge Germanium 72.64	33 As Arsenic 74.92160	34 Se Selenium 78.96	35 Br Bromine 79.904	36 Kr Krypton 83.798	
37 Rb Rubidium 85.4678	38 Sr Strontium 87.62	39 Y Yttrium 88.90585	40 Zr Zirconium 91.224	41 Nb Niobium 92.90638	42 Mo Molybdenum 95.94	43 Tc Technetium (98)	44 Ru Ruthenium 101.07	45 Rh Rhodium 102.90550	46 Pd Palladium 106.42	47 Ag Silver 107.8682	48 Cd Cadmium 112.411	49 In Indium 114.818	50 Sn Tin 118.710	51 Sb Antimony 121.760	52 Te Tellurium 127.60	53 I Iodine 126.90447	54 Xe Xenon 131.293	
55 Cs Cesium 132.90545	56 Ba Barium 137.327	57 to 71		72 Hf Hafnium 178.49	73 Ta Tantalum 180.9479	74 W Tungsten 183.84	75 Re Rhenium 186.207	76 Os Osmium 190.23	77 Ir Iridium 192.217	78 Pt Platinum 195.078	79 Au Gold 196.96655	80 Hg Mercury 200.59	81 Tl Thallium 204.3833	82 Pb Lead 207.2	83 Bi Bismuth 208.98038	84 Po Polonium (209)	85 At Astatine (210)	86 Rn Radon (222)
87 Fr Francium (223)	88 Ra Radium (226)	89 to 103		104 Rf Rutherfordium (261)	105 Db Dubnium (262)	106 Sg Seaborgium (266)	107 Bh Bohrium (264)	108 Hs Hassium (269)	109 Mt Meitnerium (268)	110 Ds Darmstadtium (271)	111 Rg Roentgenium (272)	112 Uub Ununbium (285)	113 Uut Ununtrium (284)	114 Uuq Ununquadium (289)	115 Uup Ununpentium (288)	116 Uuh Ununhexium (292)	117 Uus Ununseptium	118 Uuo Ununoctium

Alkali metals

Alkaline earth metals

Transition metals

Lanthanide series

Actinide series

Poor metals

Nonmetals

Noble gases

C

Solid

Br

Liquid

H

Gas

Tc

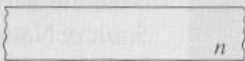
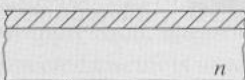
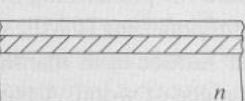
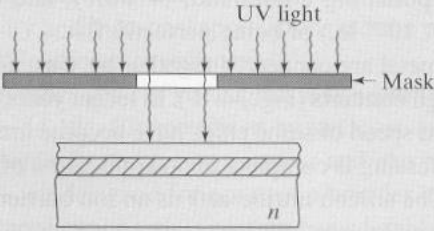
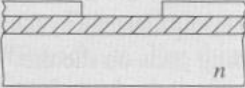
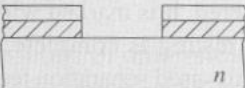
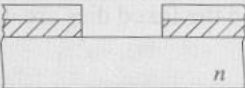
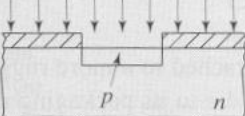
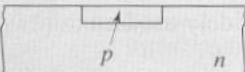
Synthetic

Atomic masses in parentheses are those of the most stable or common isotope.

Note: The subgroup numbers 1-18 were adopted in 1984 by the International Union of Pure and Applied Chemistry. The names of elements 112-118 are the Latin equivalents of those numbers.

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57 La Lanthanum 138.9055	58 Ce Cerium 140.116	59 Pr Praseodymium 140.90765	60 Nd Neodymium 144.24	61 Pm Promethium (145)	62 Sm Samarium 150.36	63 Eu Europium 151.964	64 Gd Gadolinium 157.25	65 Tb Terbium 158.92534	66 Dy Dysprosium 162.500	67 Ho Holmium 164.93032	68 Er Erbium 167.259	69 Tm Thulium 168.93421	70 Yb Ytterbium 173.04	71 Lu Lutetium 174.967
89 Ac Actinium (227)	90 Th Thorium 232.0381	91 Pa Protactinium 231.03588	92 U Uranium 238.02891	93 Np Neptunium (237)	94 Pu Plutonium (244)	95 Am Americium (243)	96 Cm Curium (247)	97 Bk Berkelium (247)	98 Cf Californium (251)	99 Es Einsteinium (252)	100 Fm Fermium (257)	101 Md Mendelevium (258)	102 No Nobelium (259)	103 Lr Lawrencium (262)

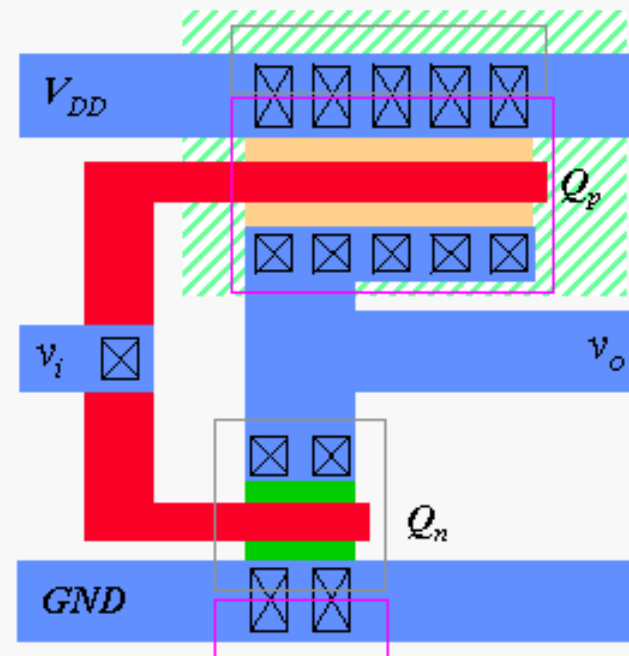
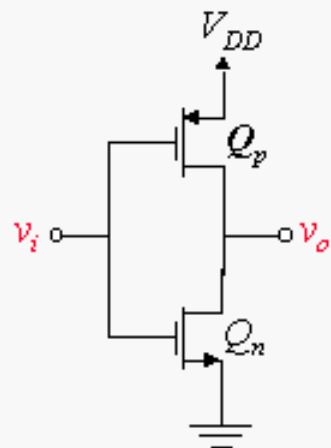
Cross-Section	Description
	Sample of <i>n</i> -type silicon
	Grow silicon dioxide by oxidation.
	Apply photoresist.
	Expose photoresist using appropriate lithographic mask.
	Develop photoresist.
	Etch silicon dioxide.
	Remove photoresist.
	Implant boron.
	Remove silicon dioxide.

Processing of a p-Type Region in n-Type Silicon

pn junction diode

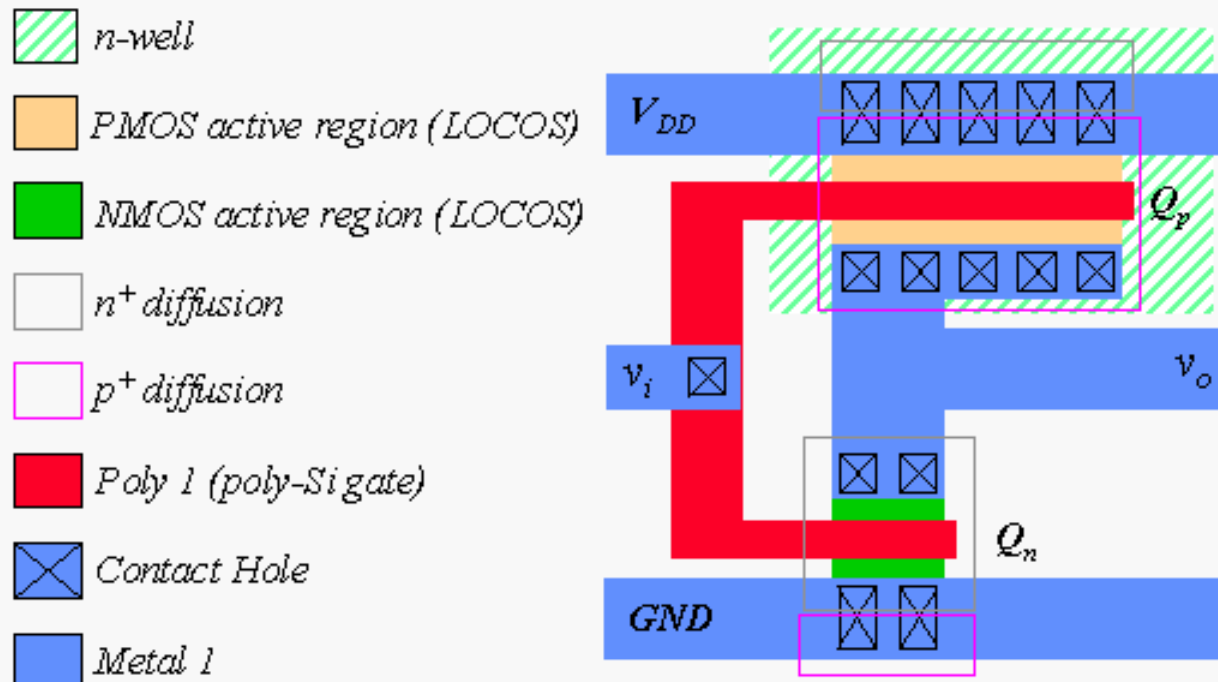


PHYSICAL LAYOUT OF CMOS INVERTER





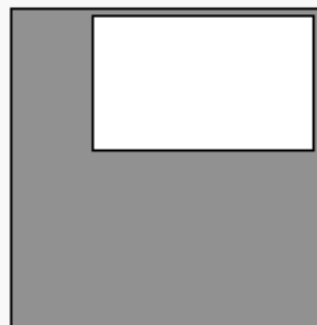
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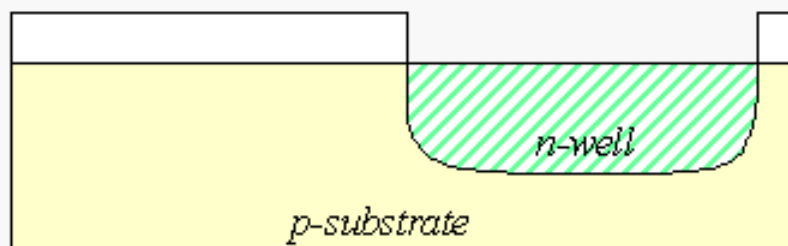
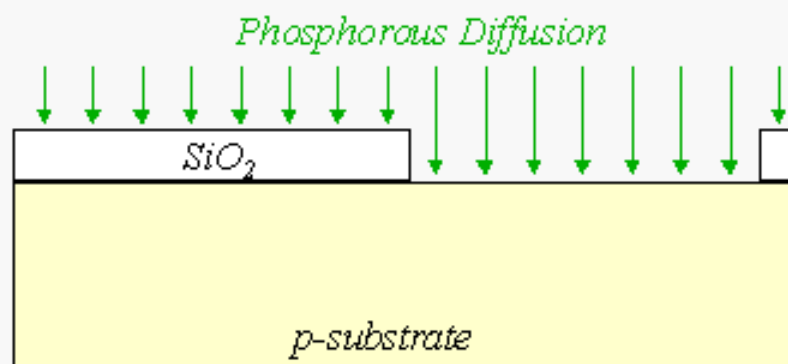


N-WELL DIFFUSION

- SiO_2 is etched using Mask 1.



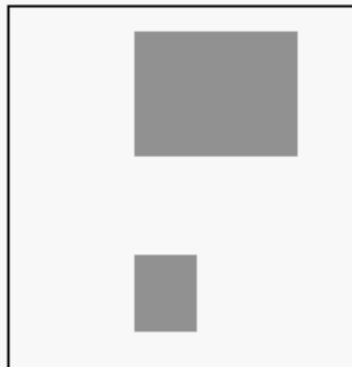
- Phosphorous is diffused into the unmasked regions of silicon creating an n-well for the fabrication of p-channel devices



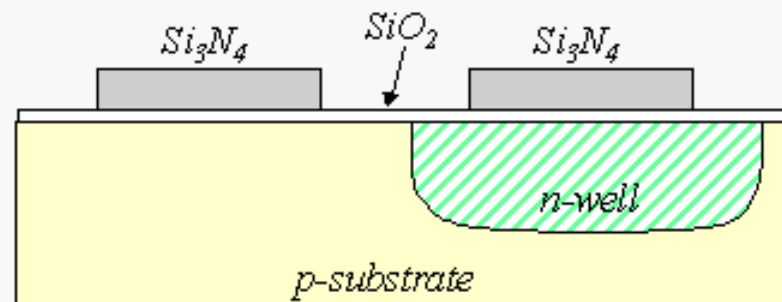


DEFINE ACTIVE REGIONS

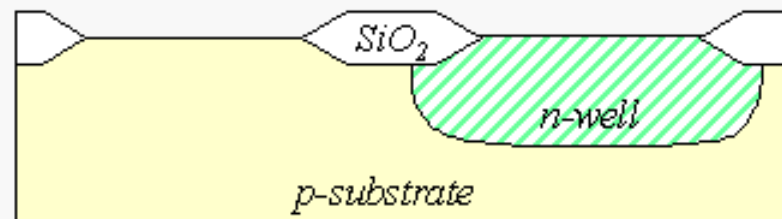
- Mask 2 creates the active regions where the MOSFETs will be placed



- Local oxidation provides isolation between the MOSFETs



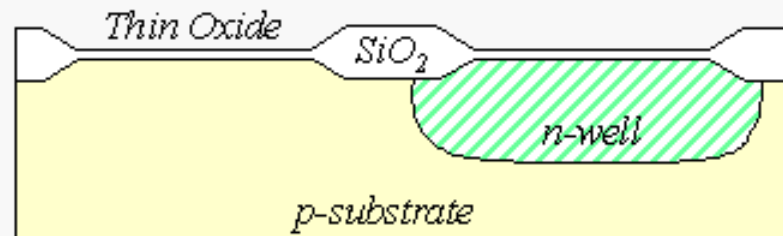
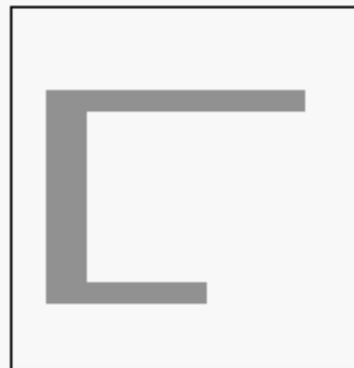
A thick field oxide will be grown using a wet oxidation step process called local oxidation (LOCOS).



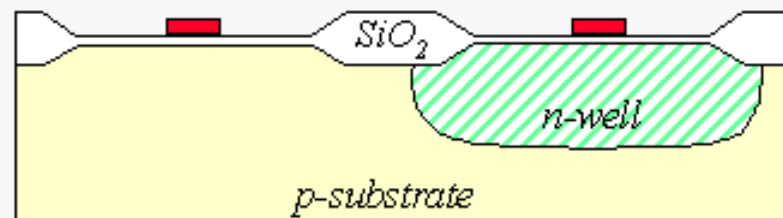


POLYSILICON GATE

- A high quality thin oxide is grown in the active area ($\sim 0.1 \mu\text{m}$)
- *Mask 3* is used to deposit the polysilicon gate (*most critical step*)



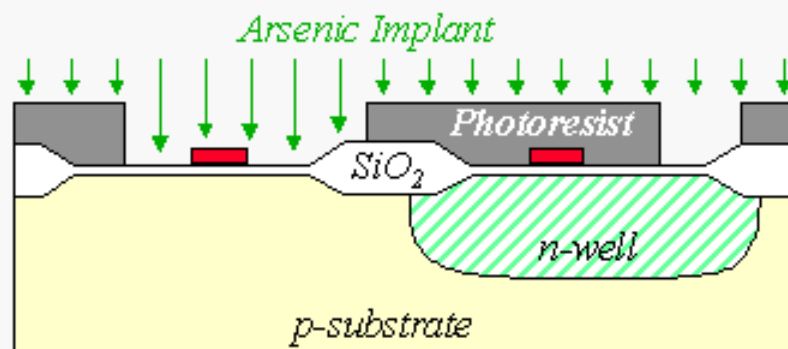
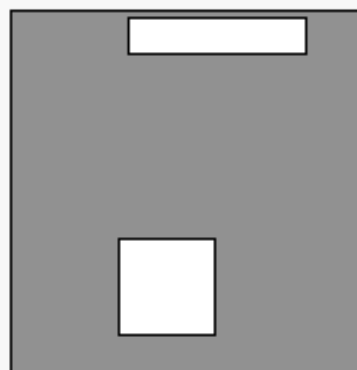
The polysilicon layer is usually arsenic doped (n-type). The photolithography in this step is the most demanding since it requires the finest resolution to create the narrow MOS channels.



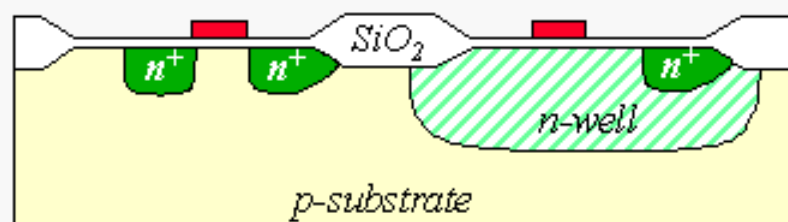


n^+ DIFFUSION

- *Mask 4* is used to control a heavy arsenic implant and create the source and drain of the n-channel devices.
- This is a self-aligned structure.



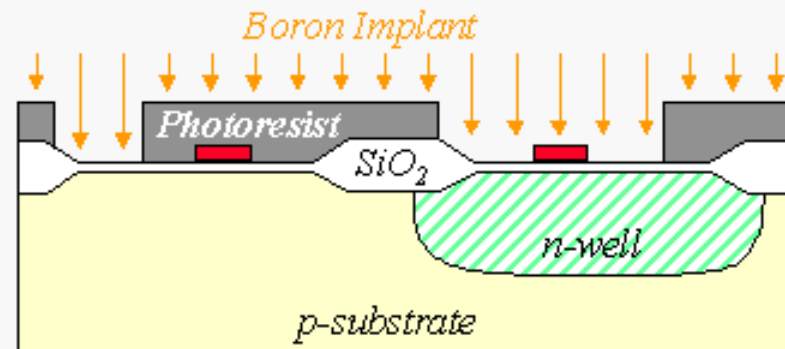
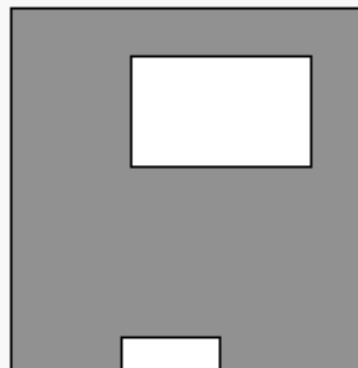
The polysilicon gate acts like a barrier for this implant to protect the channel region.



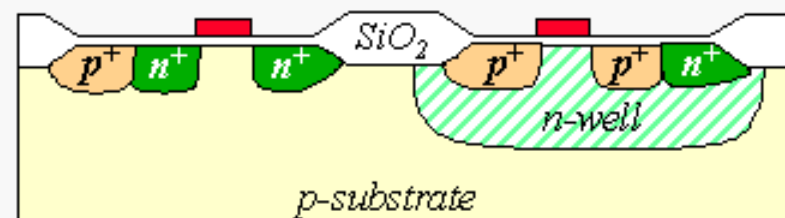


p^+ DIFFUSION

- *Mask 5* is used to control a heavy Boron implant and create the source and drain of the n-channel devices.
- This is a self-aligned structure.



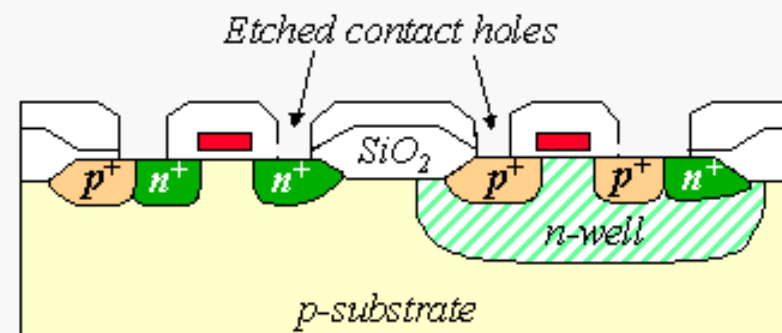
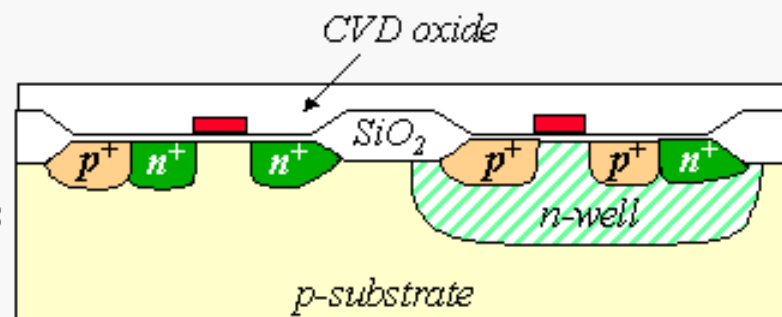
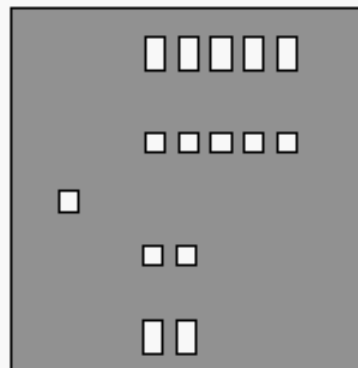
The polysilicon gate acts like a barrier for this implant to protect the channel region.





CONTACT HOLES

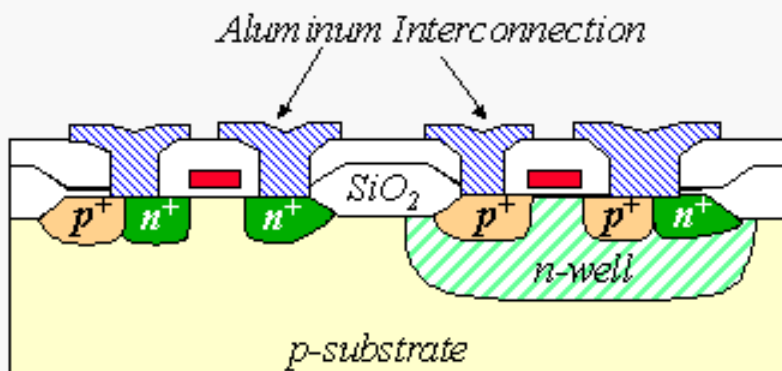
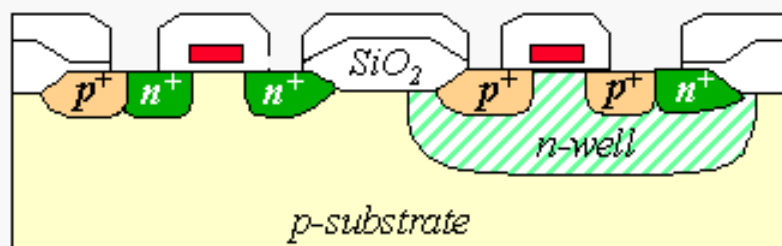
- A thin layer of CVD oxide is deposited over the entire wafer
- Mask σ is used to pattern the contact holes
- Etching opens the holes.





METALIZATION

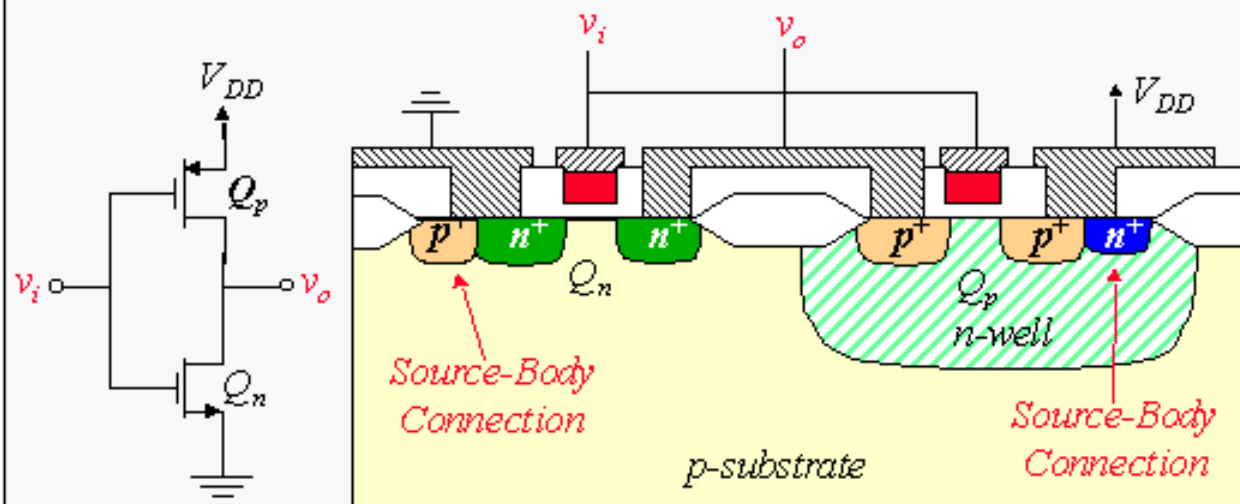
- A thin layer of aluminum is evaporated or sputtered onto the wafer.
- Mask 7 is used to pattern the interconnection.





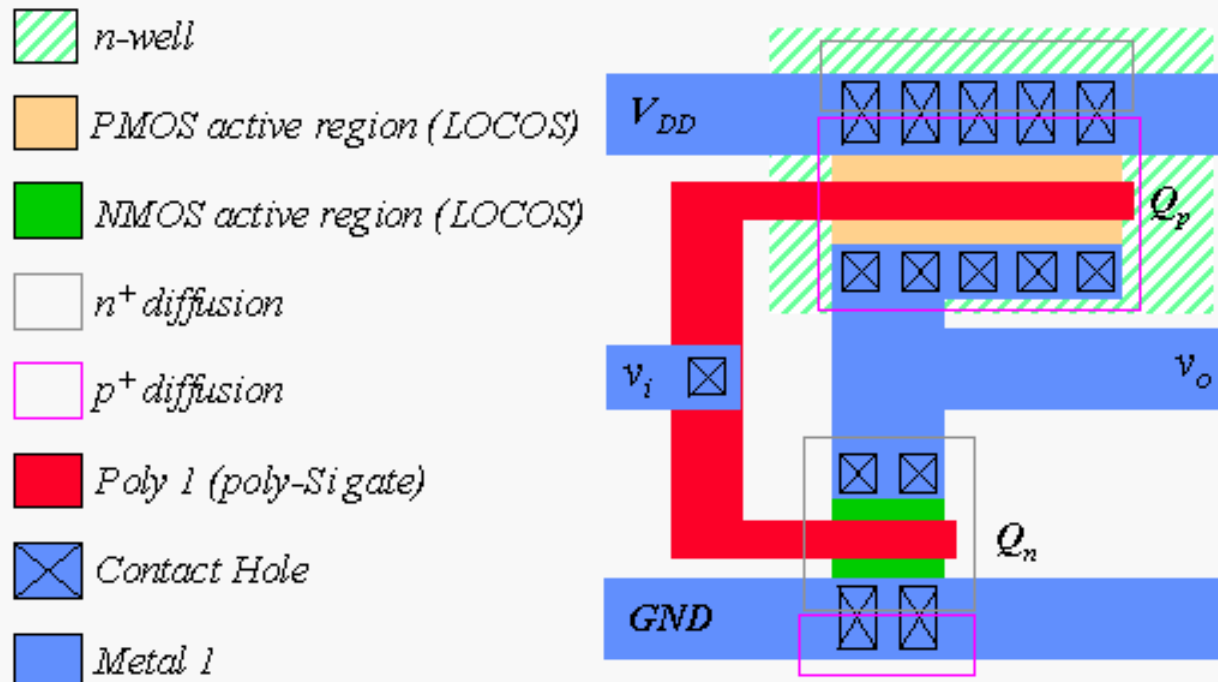
PHYSICAL LAYOUT OF CMOS INVERTER

Side View





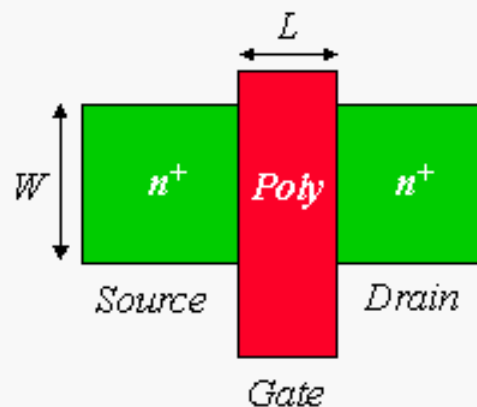
PHYSICAL LAYOUT OF CMOS INVERTER



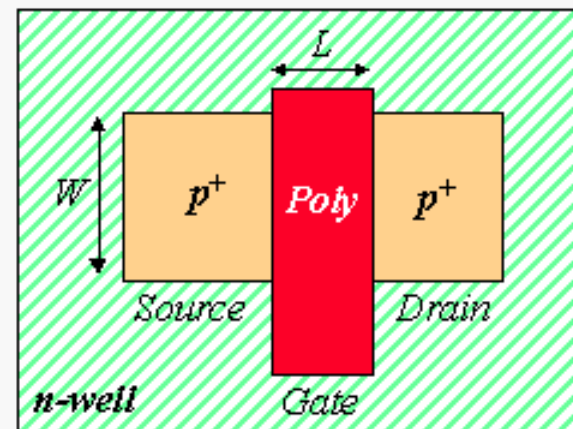


MOSFET LAYOUT

Top View



n-channel MOSFET



p-channel MOSFET

End